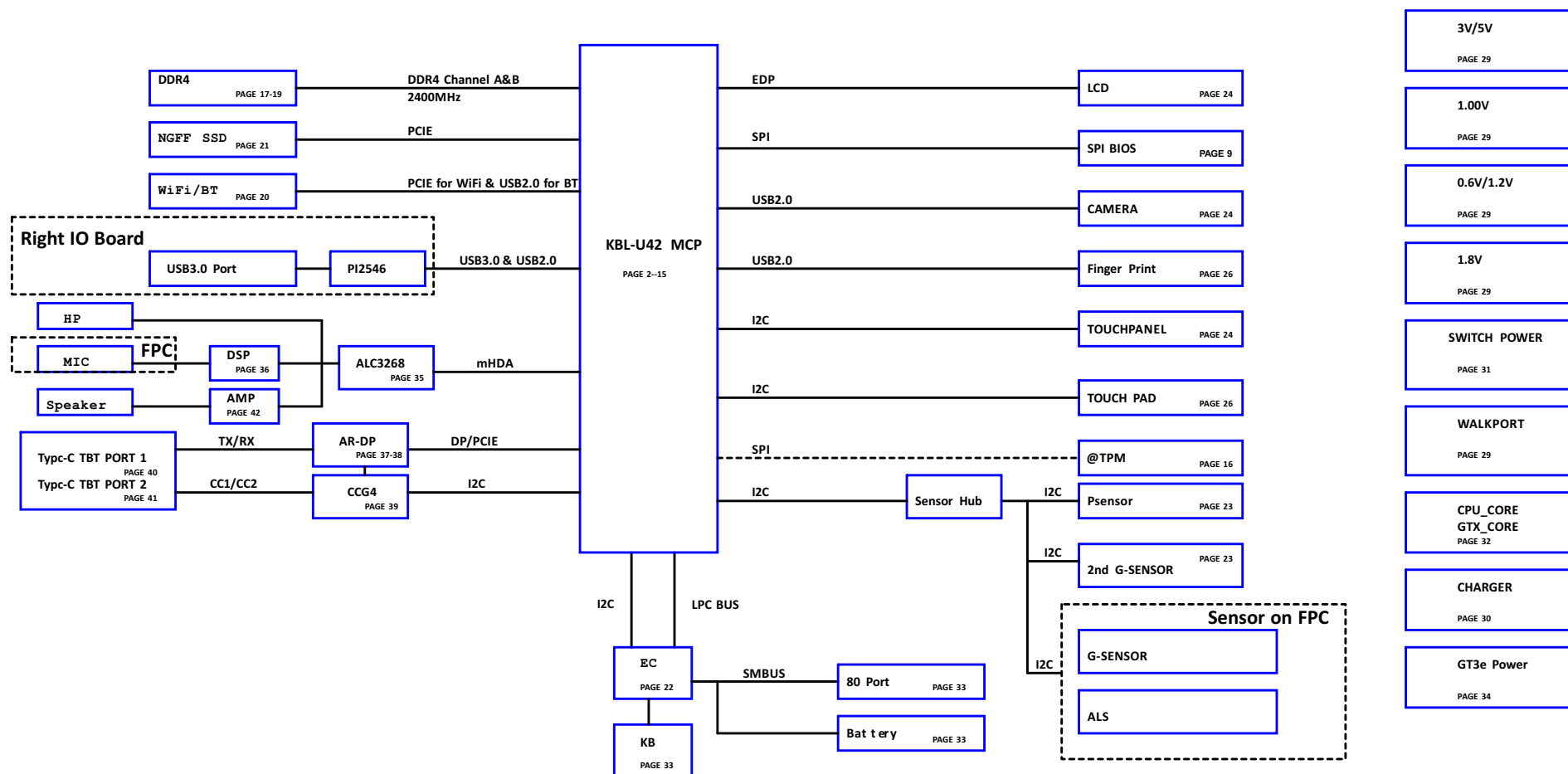
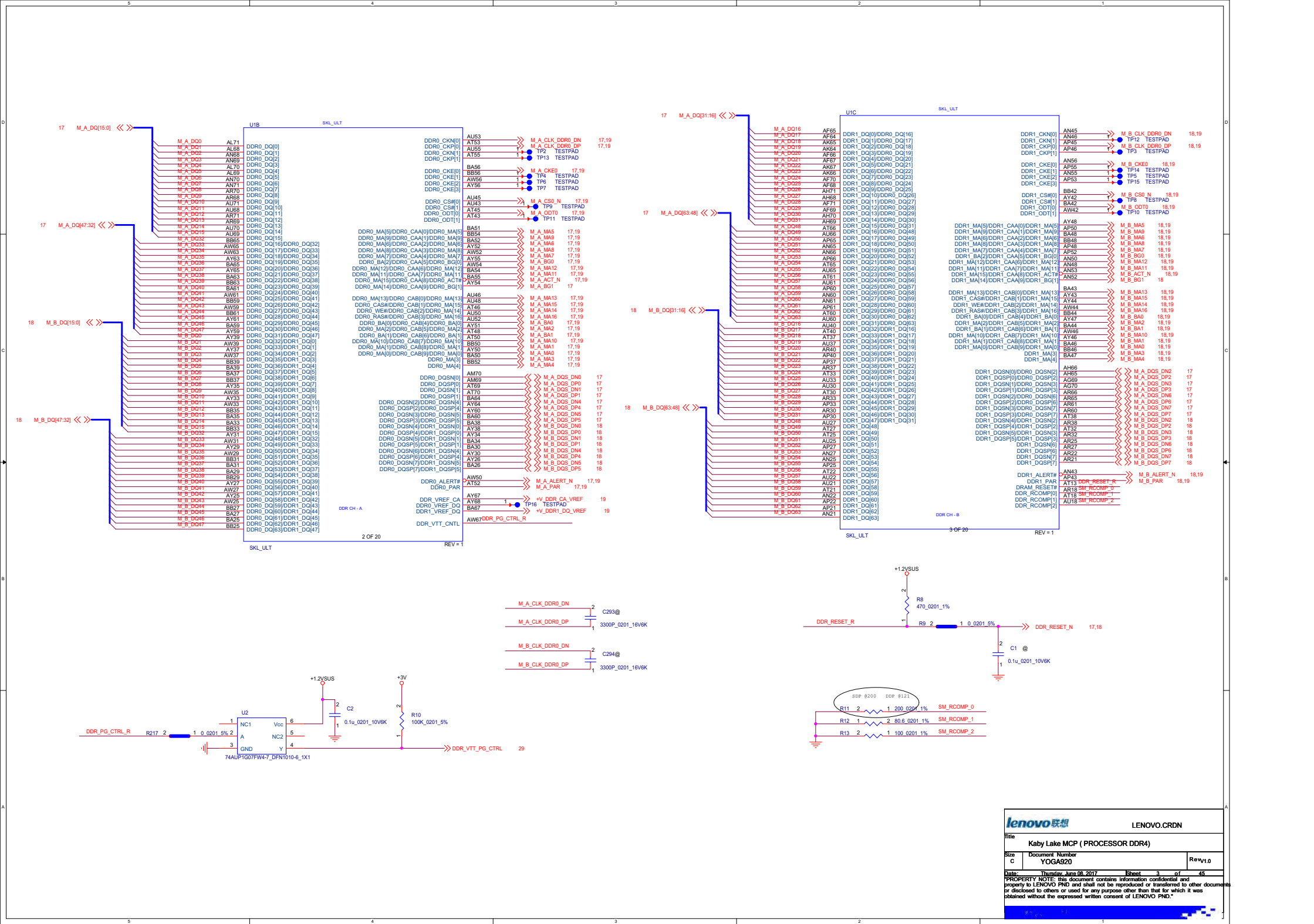
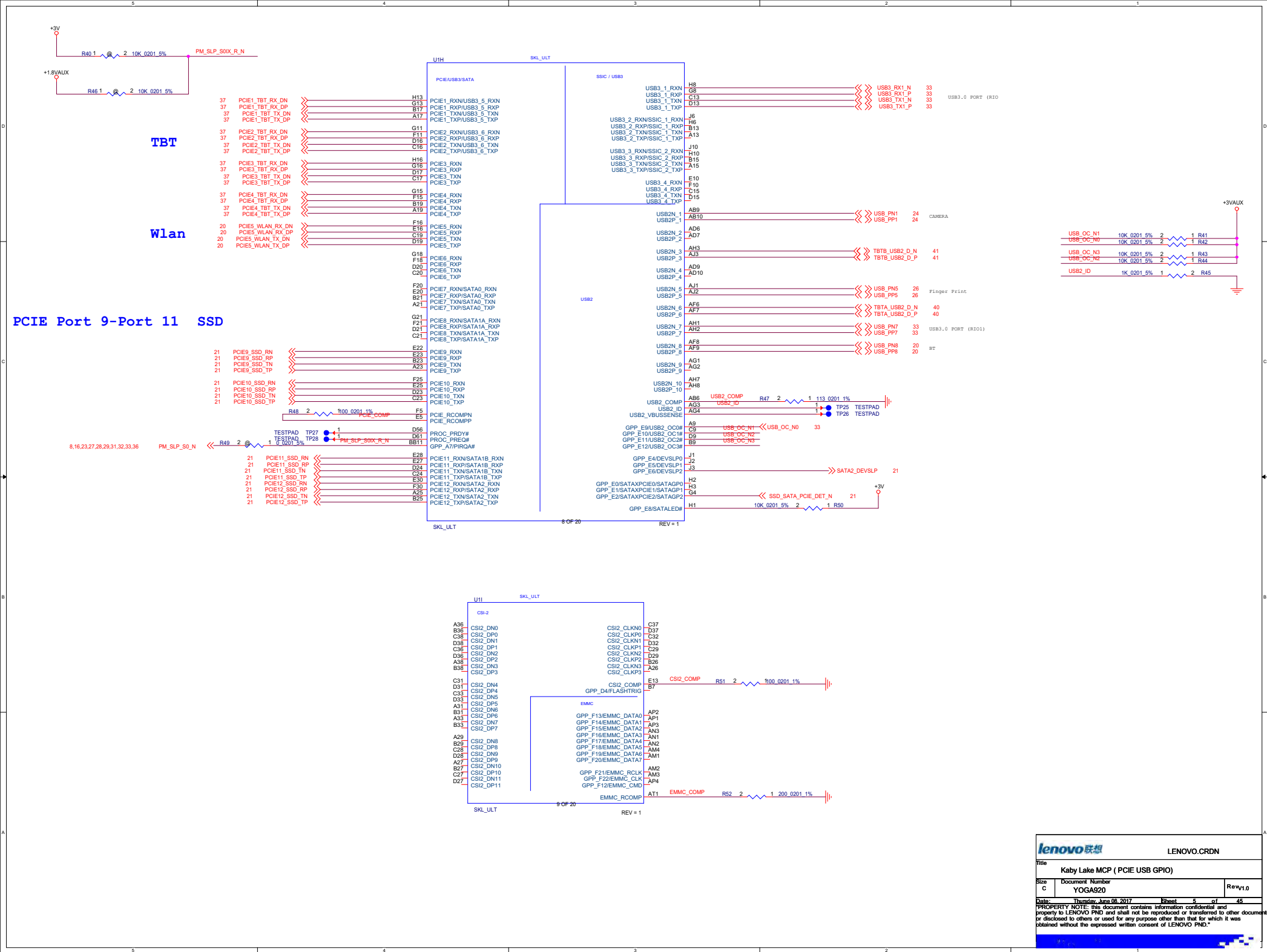
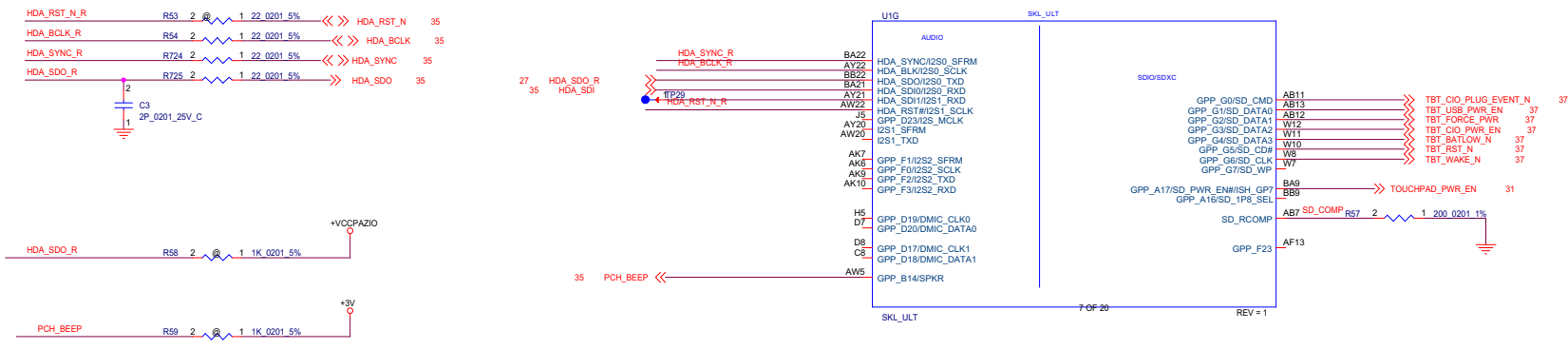


Yoga920 KBL-U42 SIT Schematic Block Diagram









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Title

Kaby Lake MCP (HDA/I2S/SDIO/DMIC)

Size

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YOGA920

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Date:

Thursday, June 08, 2017

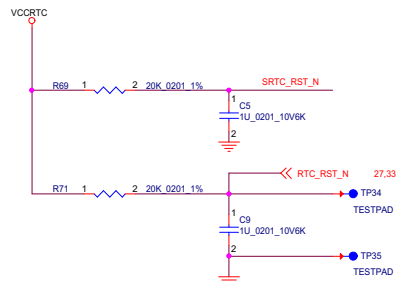
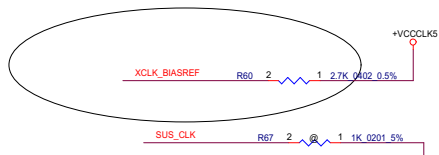
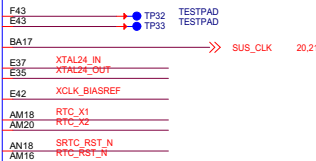
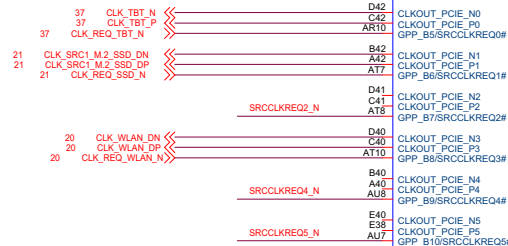
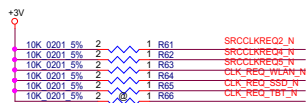
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of

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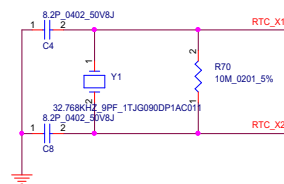
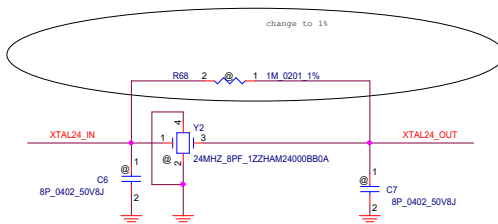
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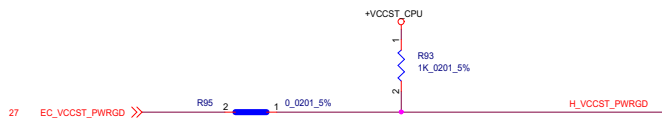
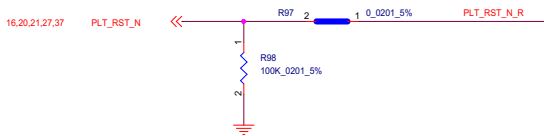
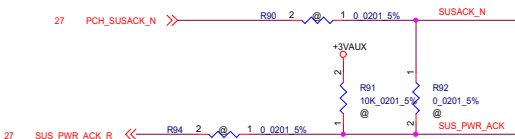
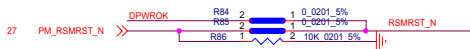
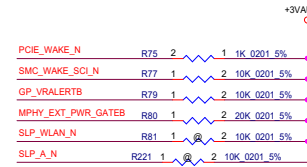
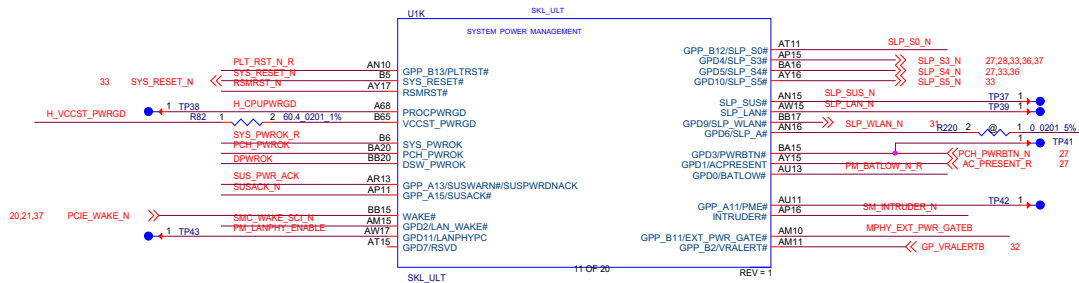
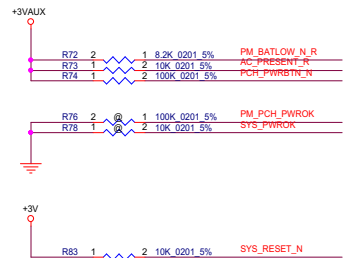


ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

Need to put on the bottom





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Title

Kaby Lake MCP (PM)

Size

C

Document Number

YOGA920

Rev

V1.0

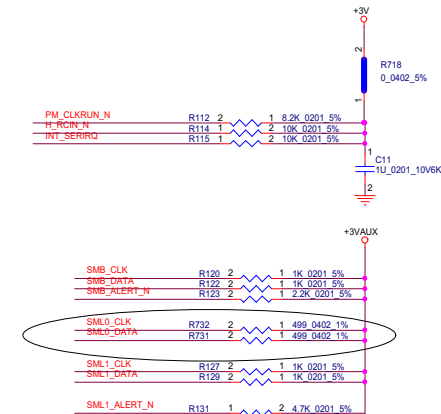
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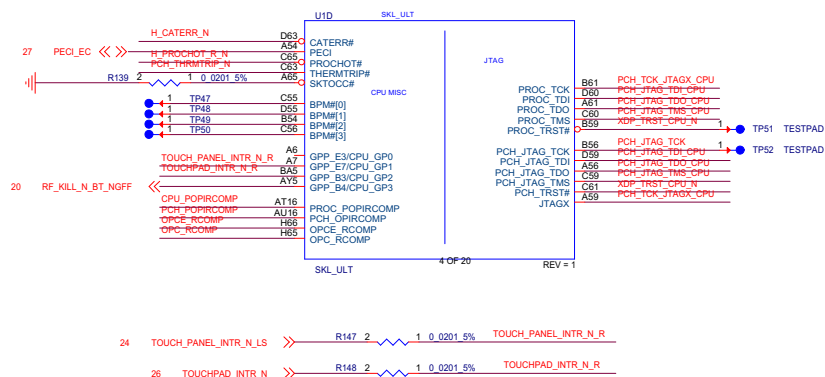
Thursday, June 08, 2017

Sheet

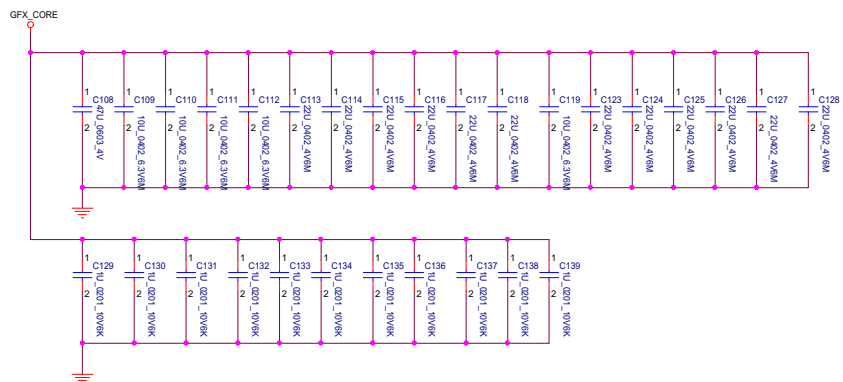
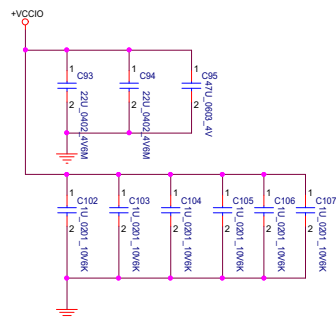
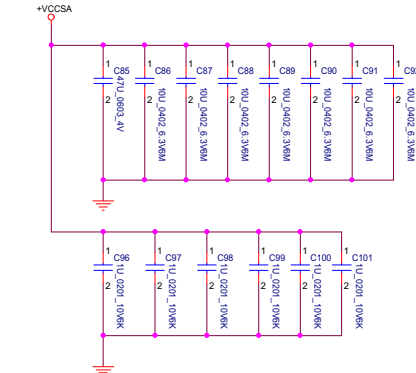
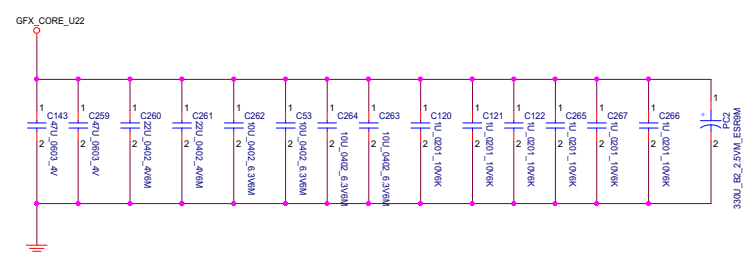
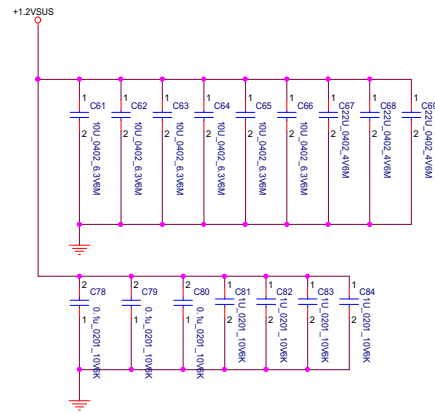
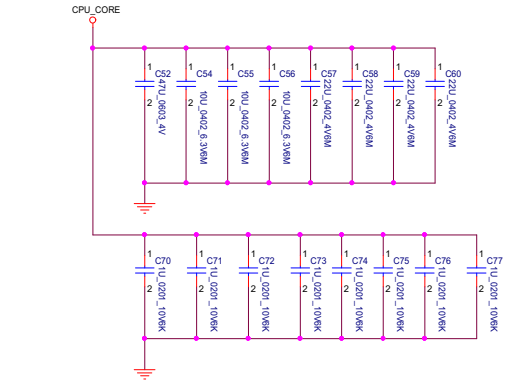
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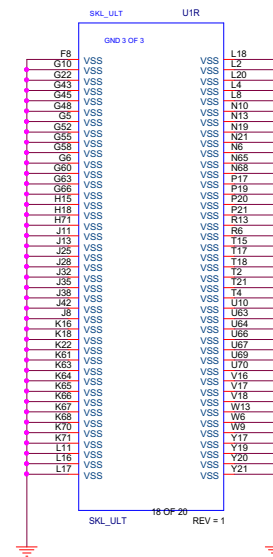
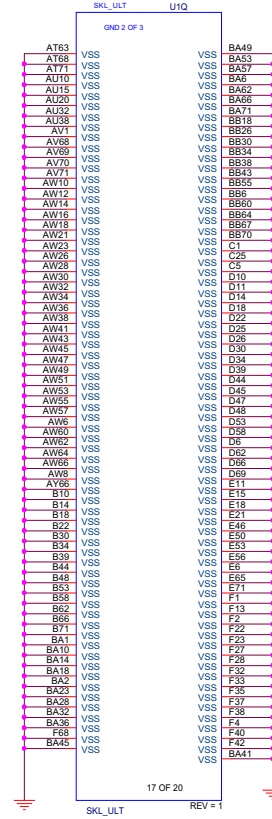
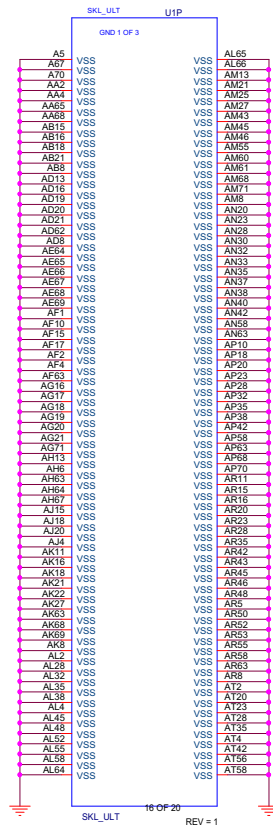
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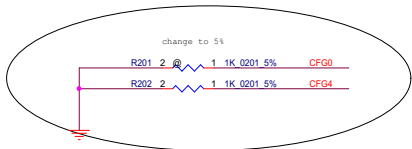


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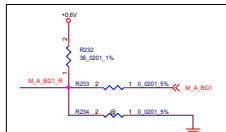
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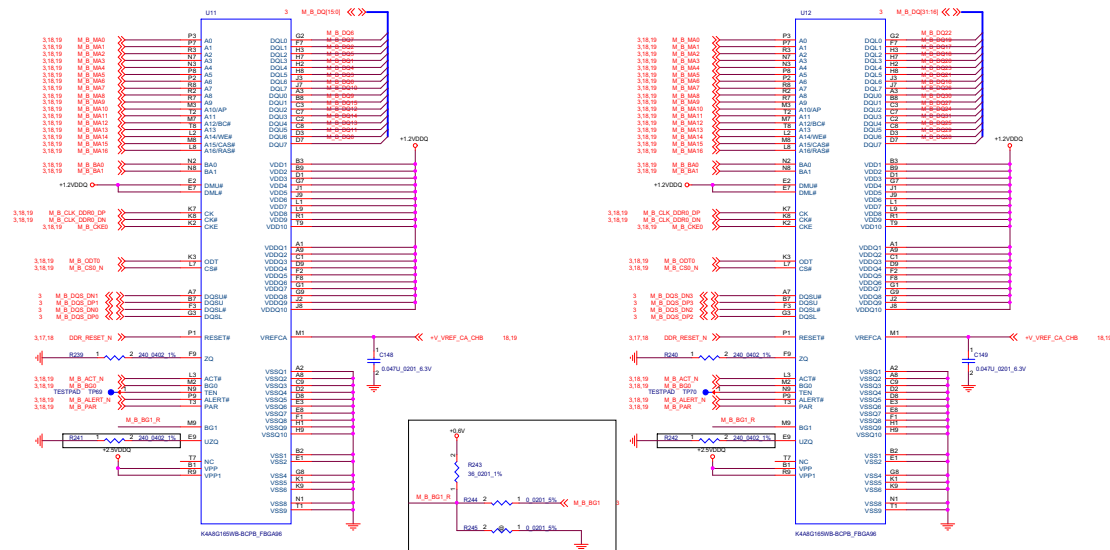
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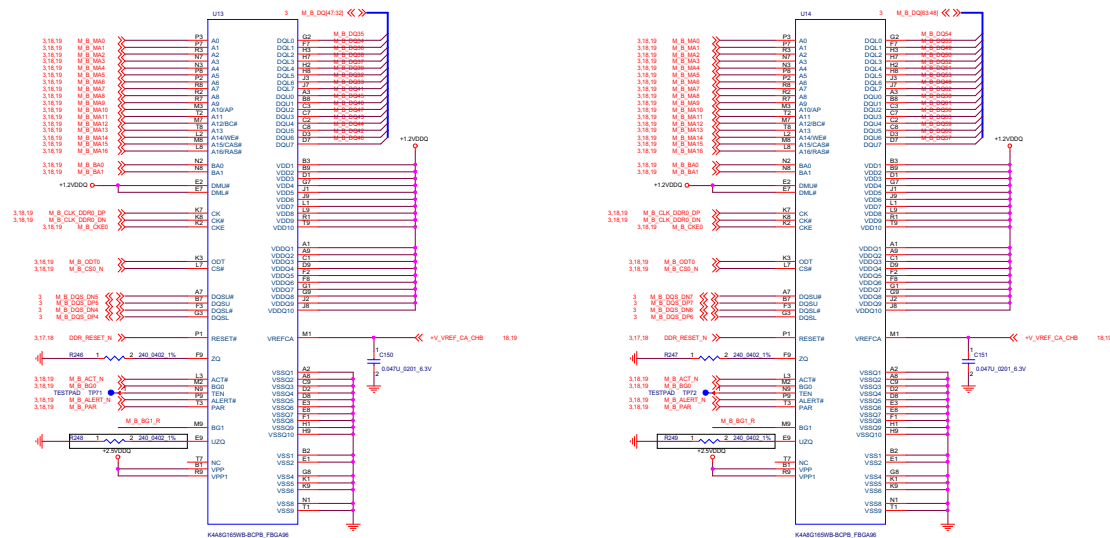


The PCB layout for the SKL_ULT board features a central U15 microcontroller. The layout includes various test pads (TP57, TP58, TP59, TP60, TP61, TP62, TP63, TP64) and configuration pins (CFG0, CFG4, ITP_PMODE). The U15 is connected to a network of resistors (R203, R204, R205, R206, R777, R776, R102) and capacitors (C141, C142, C69, C71, F60, F65, F61). The board also includes a 24MHz crystal (Y3) and a 1.2V regulator (R206). The layout is labeled with SKL_ULT and REV = 1.

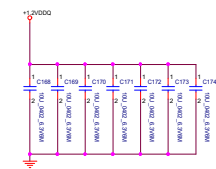
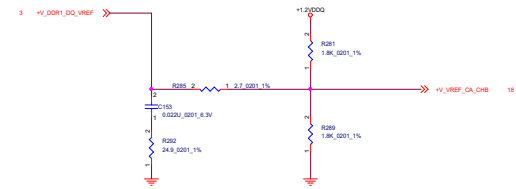


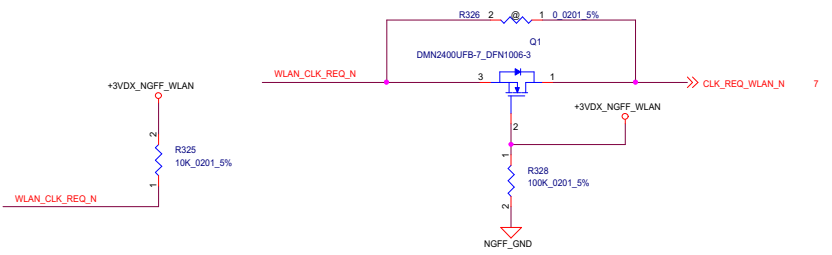
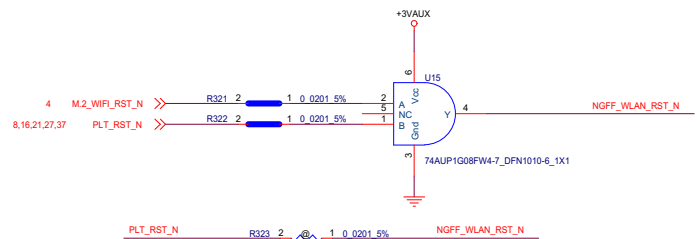
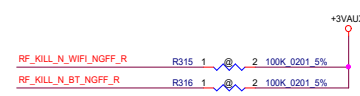
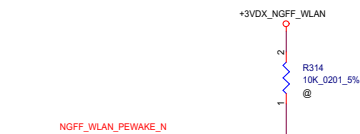
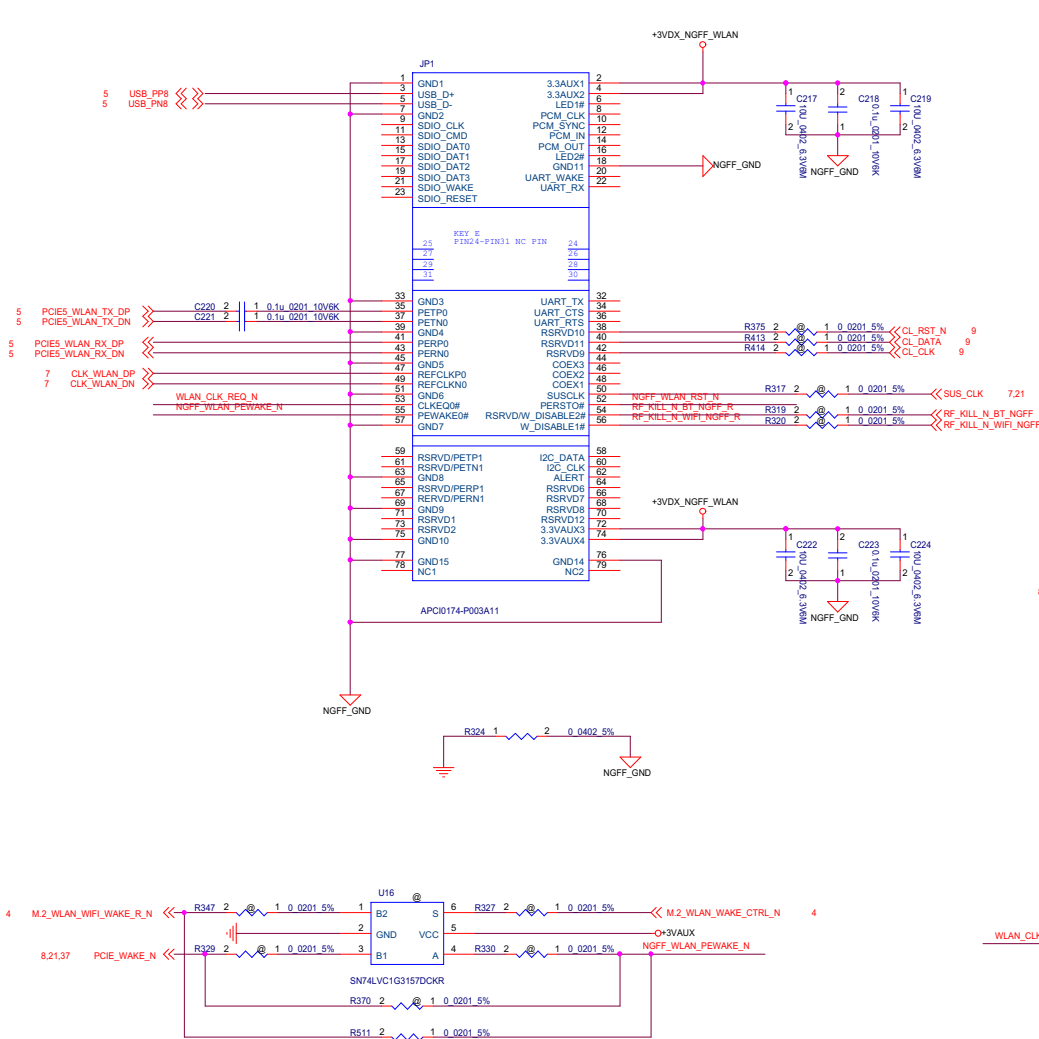


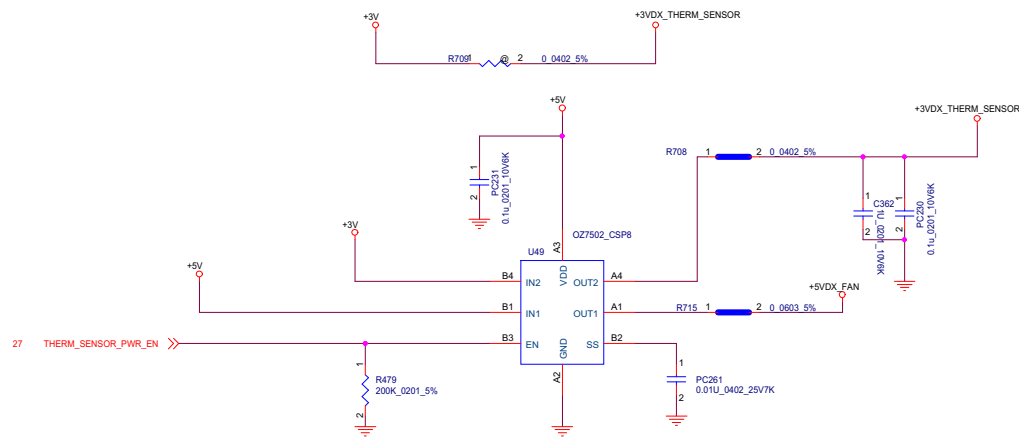
DDP: Stuff R244 and R243, Dummy R245; R241 242 248 249 @ 240ohm
SDP: Dummy R244 and R243, Stuff R245; R241 242 248 249@ 0ohm



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Doc	YOGA820	Rev	1.0
D	YOGA820	Rev	1.0
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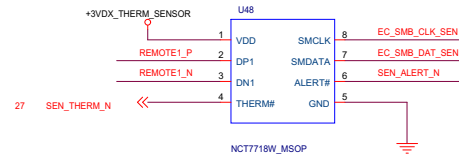
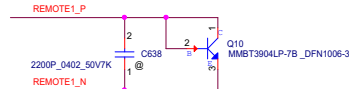




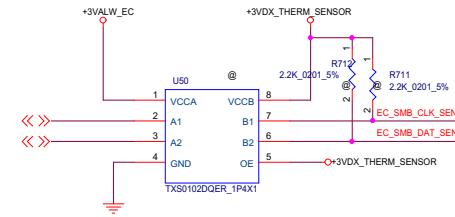
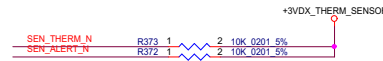
21,22,24,27,29,30,32,33 EC_SMB_CLK << >> R716 2 1 0.0201 5% EC_SMB_CLK_SEN
21,22,24,27,29,30,32,33 EC_SMB_DAT << >> R717 2 1 0.0201 5% EC_SMB_DAT_SEN

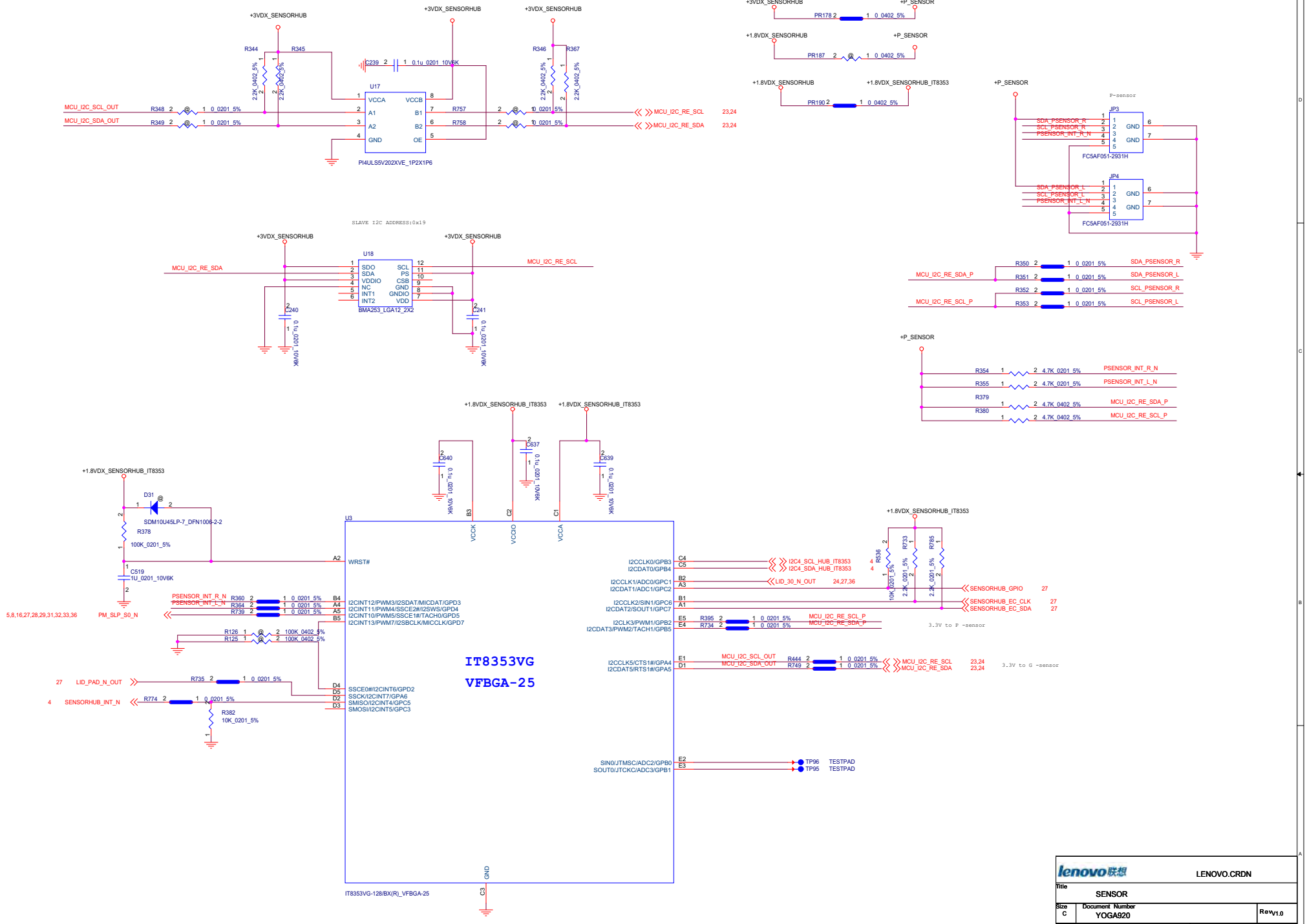
BRD Note:
Placed close to NCT7718W_MSOP

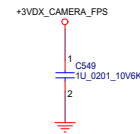
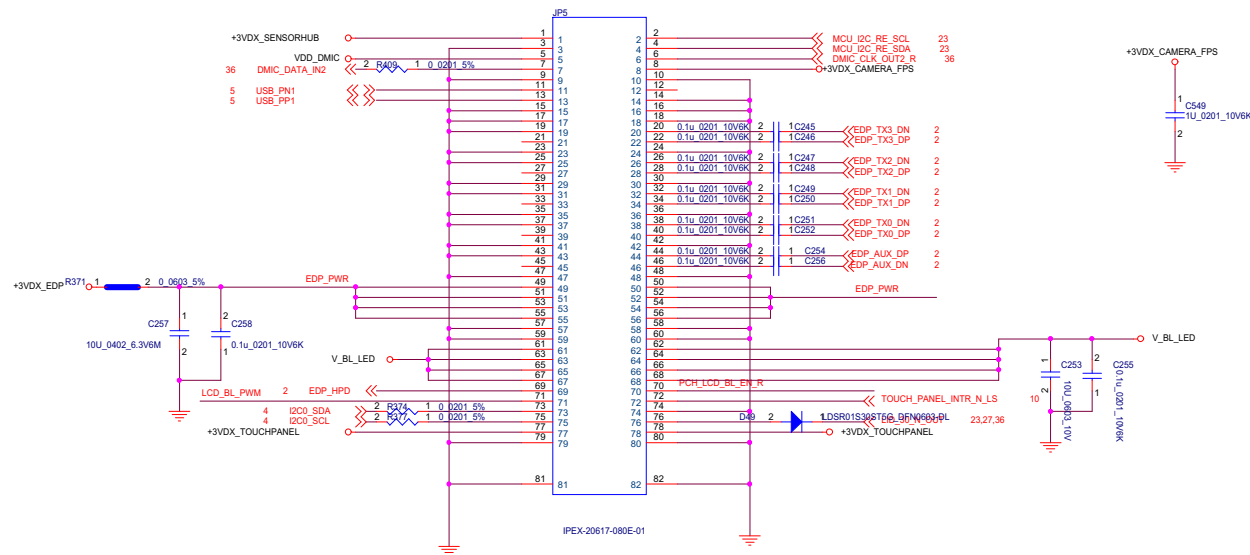
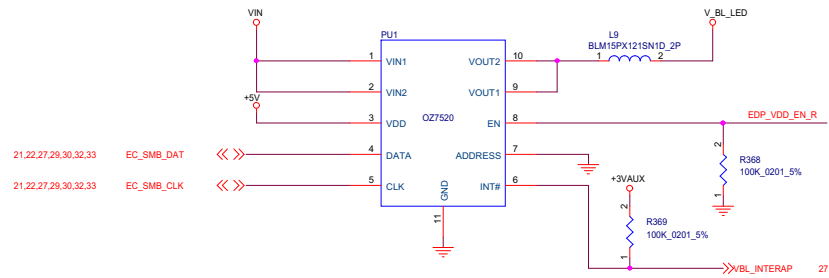
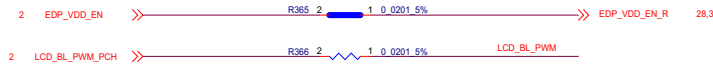
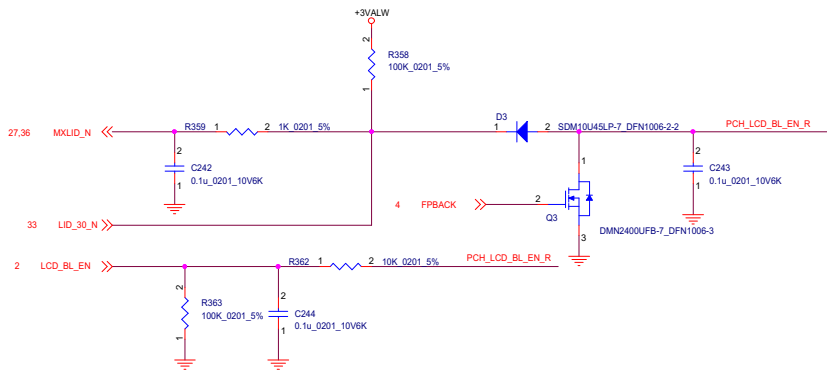
BRD Note:
Placed close to
W/S=10:10




SMBus ADDRESS:1001_100xb







5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Title

RESERVE

Size

Document Number

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YOGA920

V1.0

Date:

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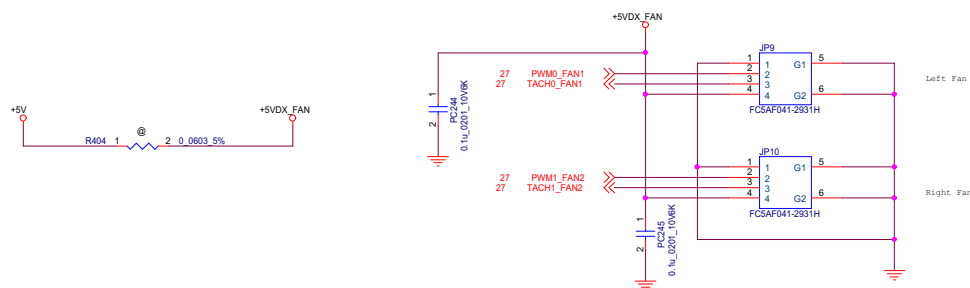
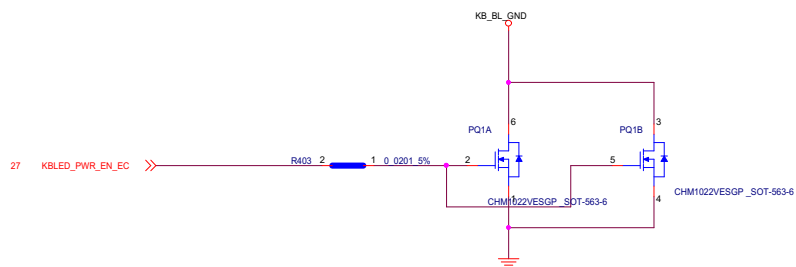
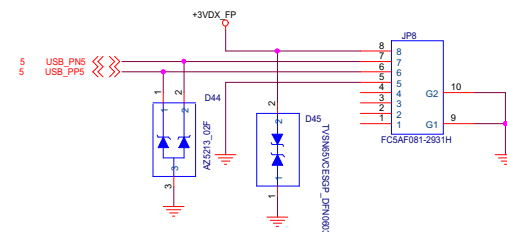
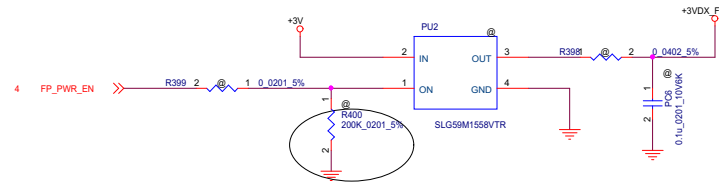
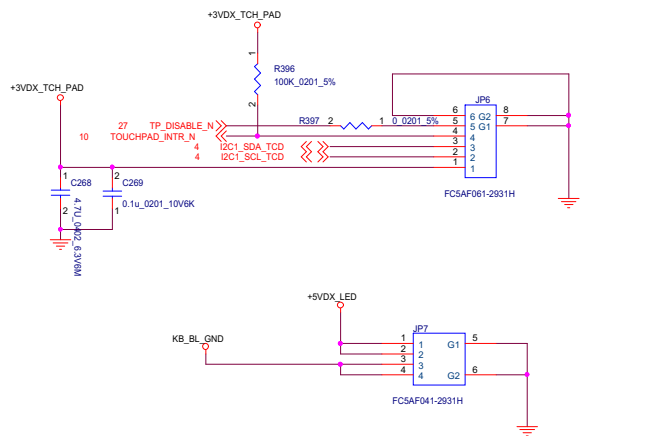
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TP/FP/KB LED

Size

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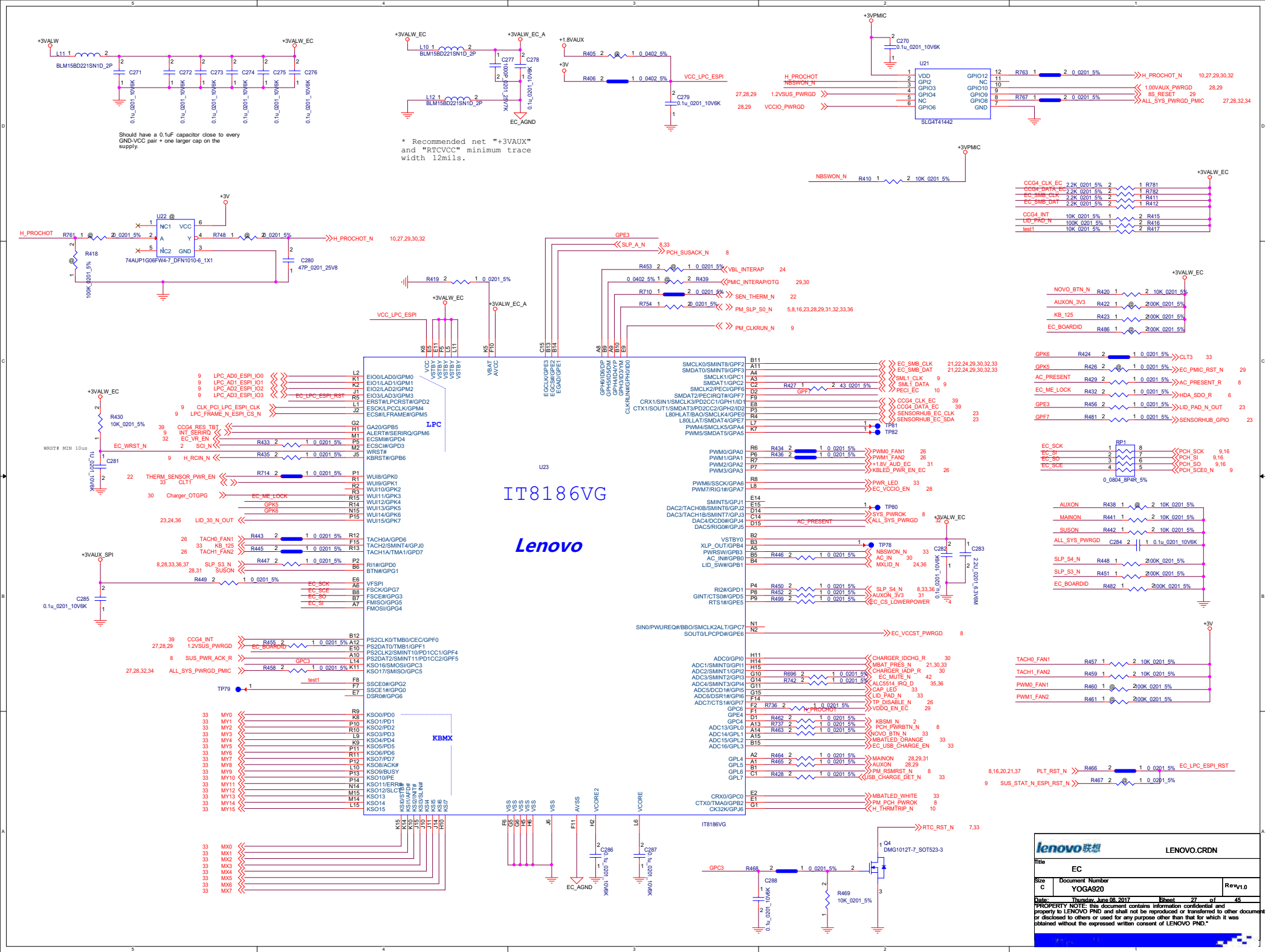
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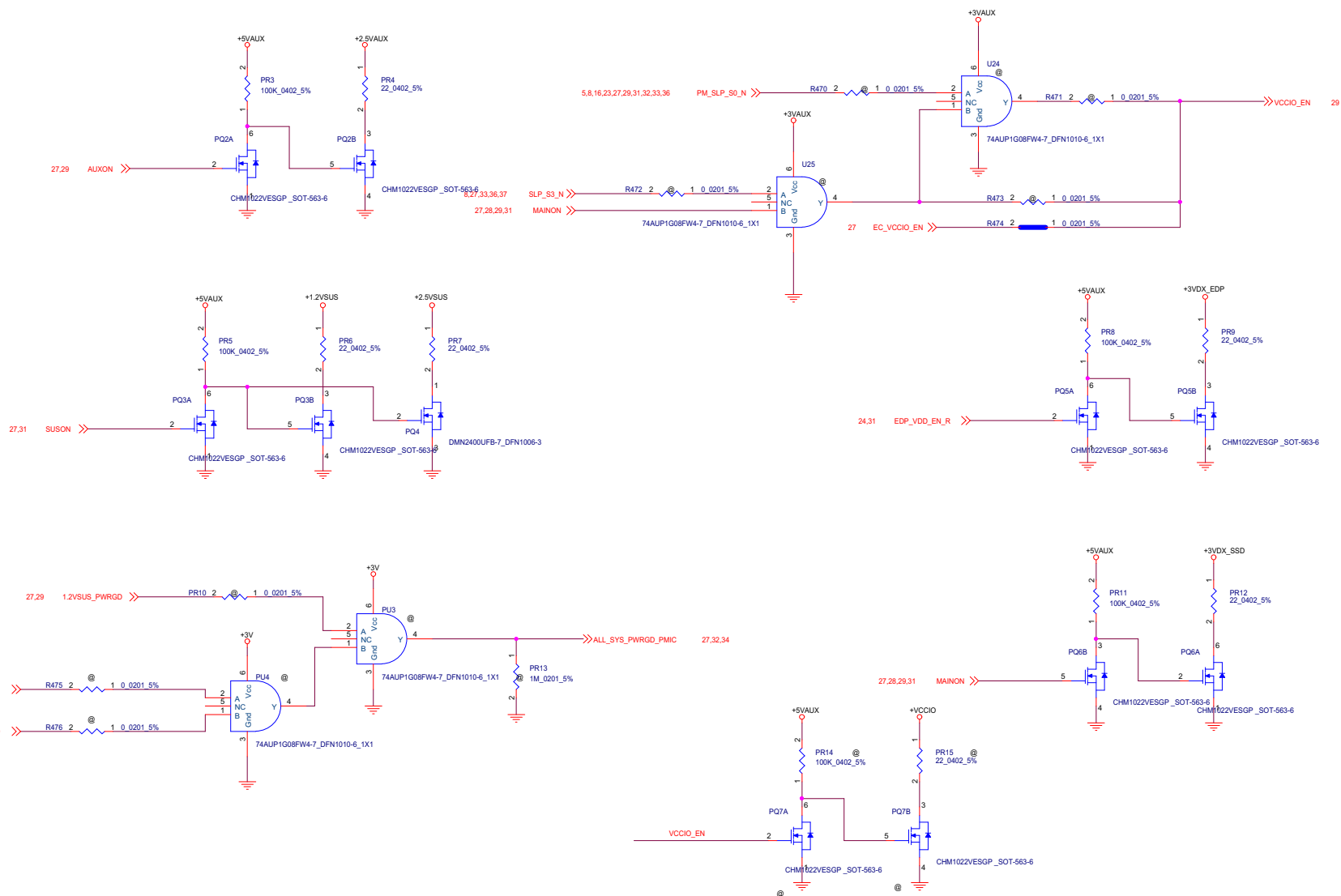
Thursday, June 08, 2017

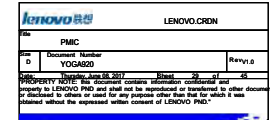
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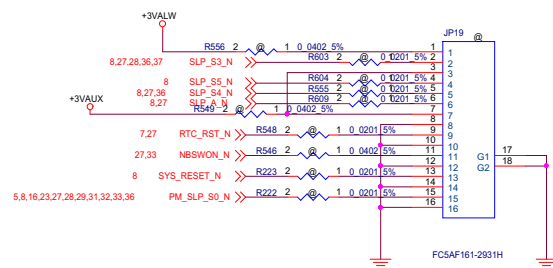
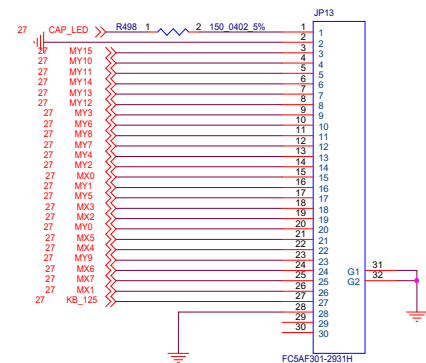
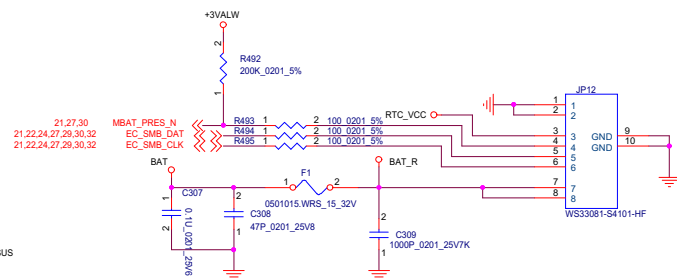
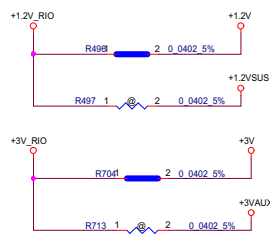
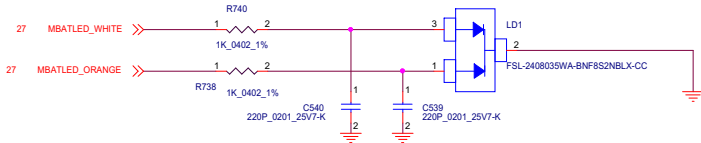
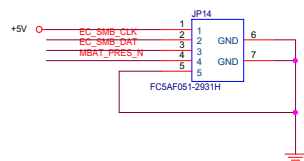
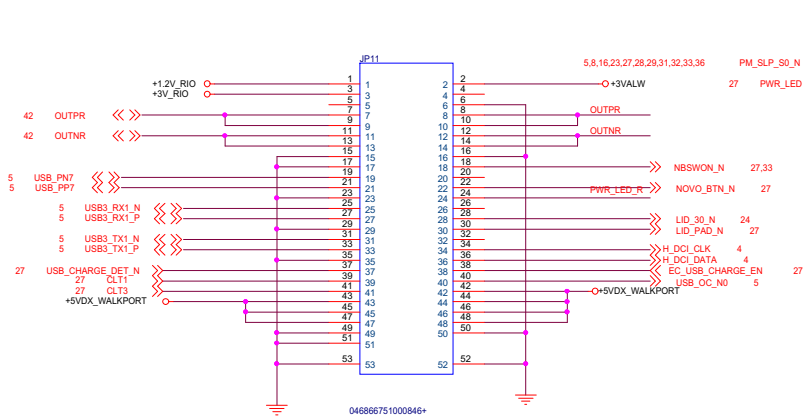
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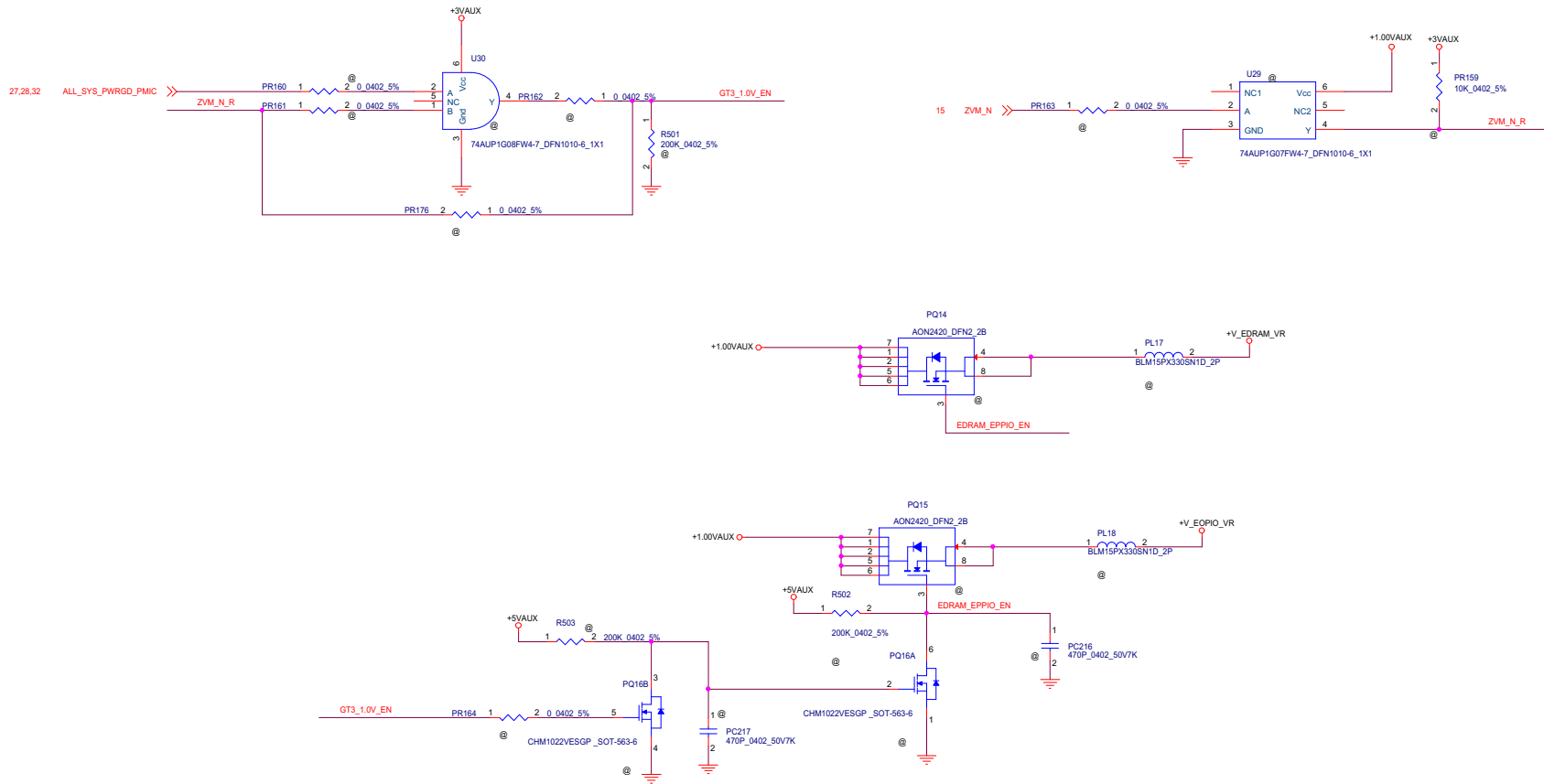
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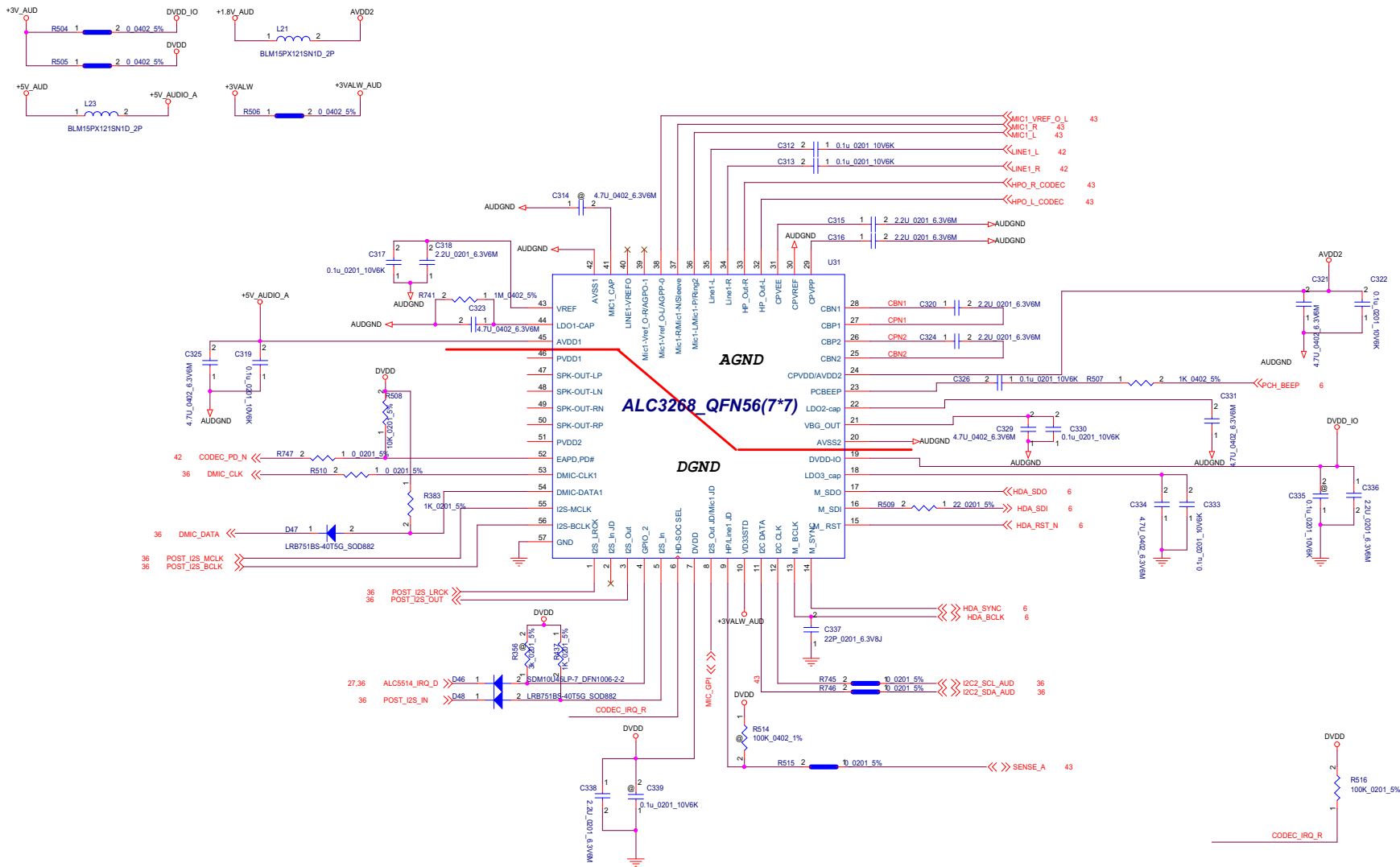




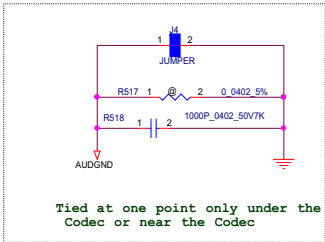


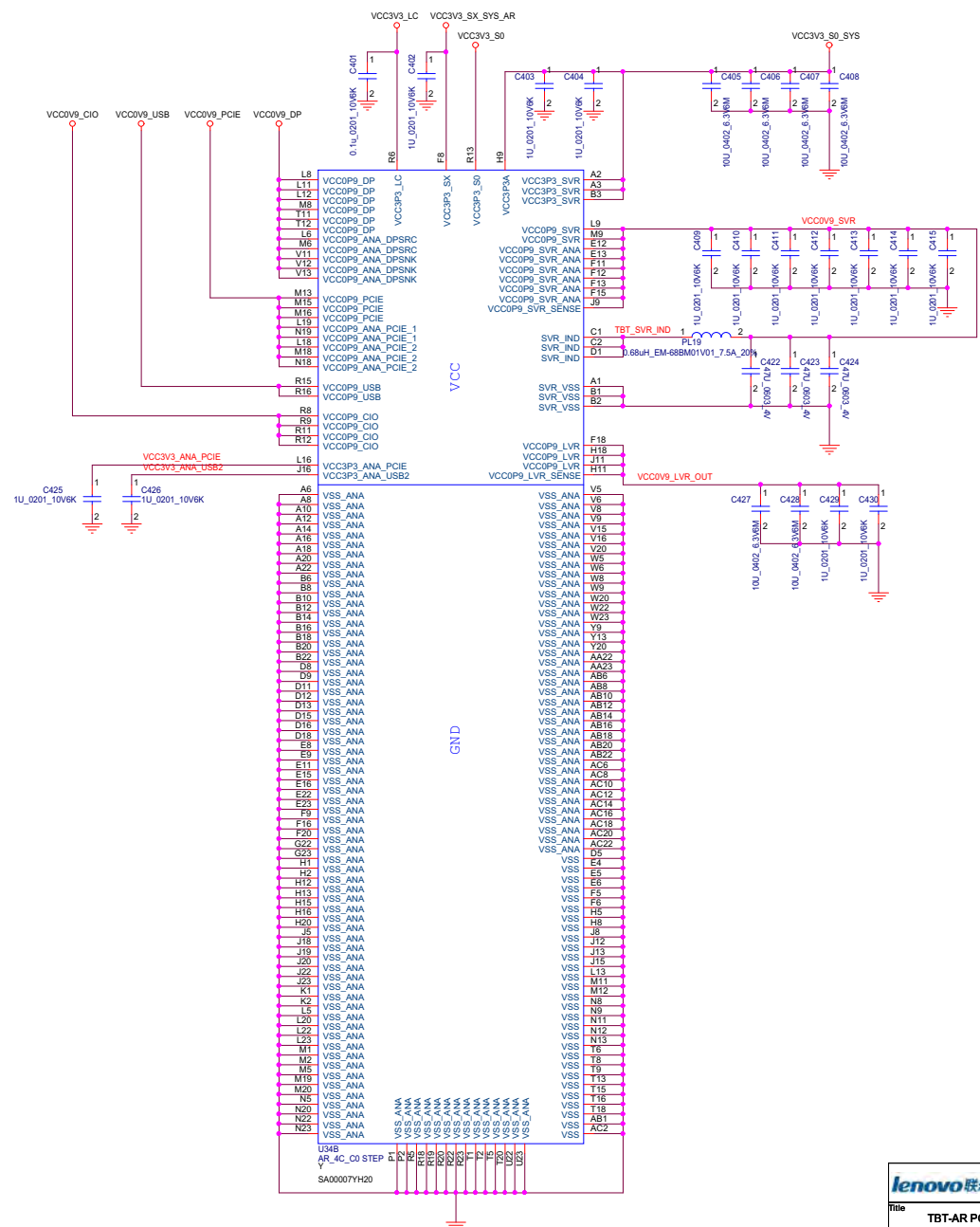
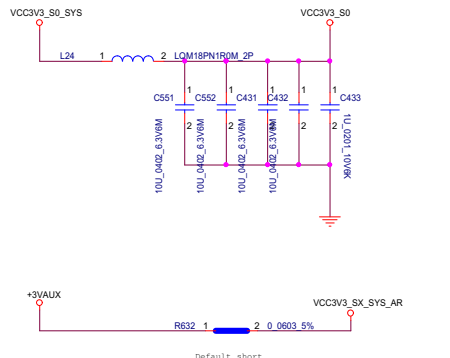
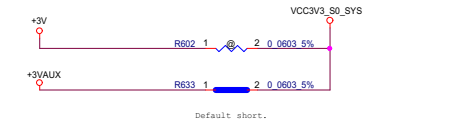
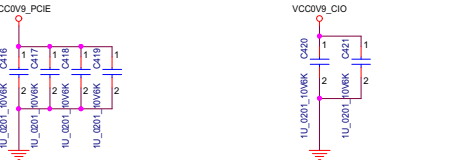
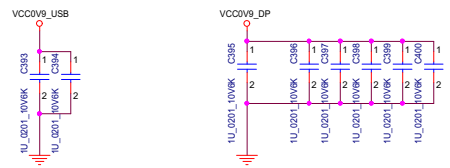


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Title			
VCCOPC			
Size	Document Number		Rev
C	YOGA920		v1.0
Date:	Thursday, June 08, 2017	Sheet	34 of 45
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PIN6 is for HDA and I2S strap pin.
High is HDA enable. (Default)
Low is I2S enable.





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Title

TBT-AR POWER

Size

C

Document Number

YOGA 920

Rev

0.3

Date

Thursday, June 08, 2017

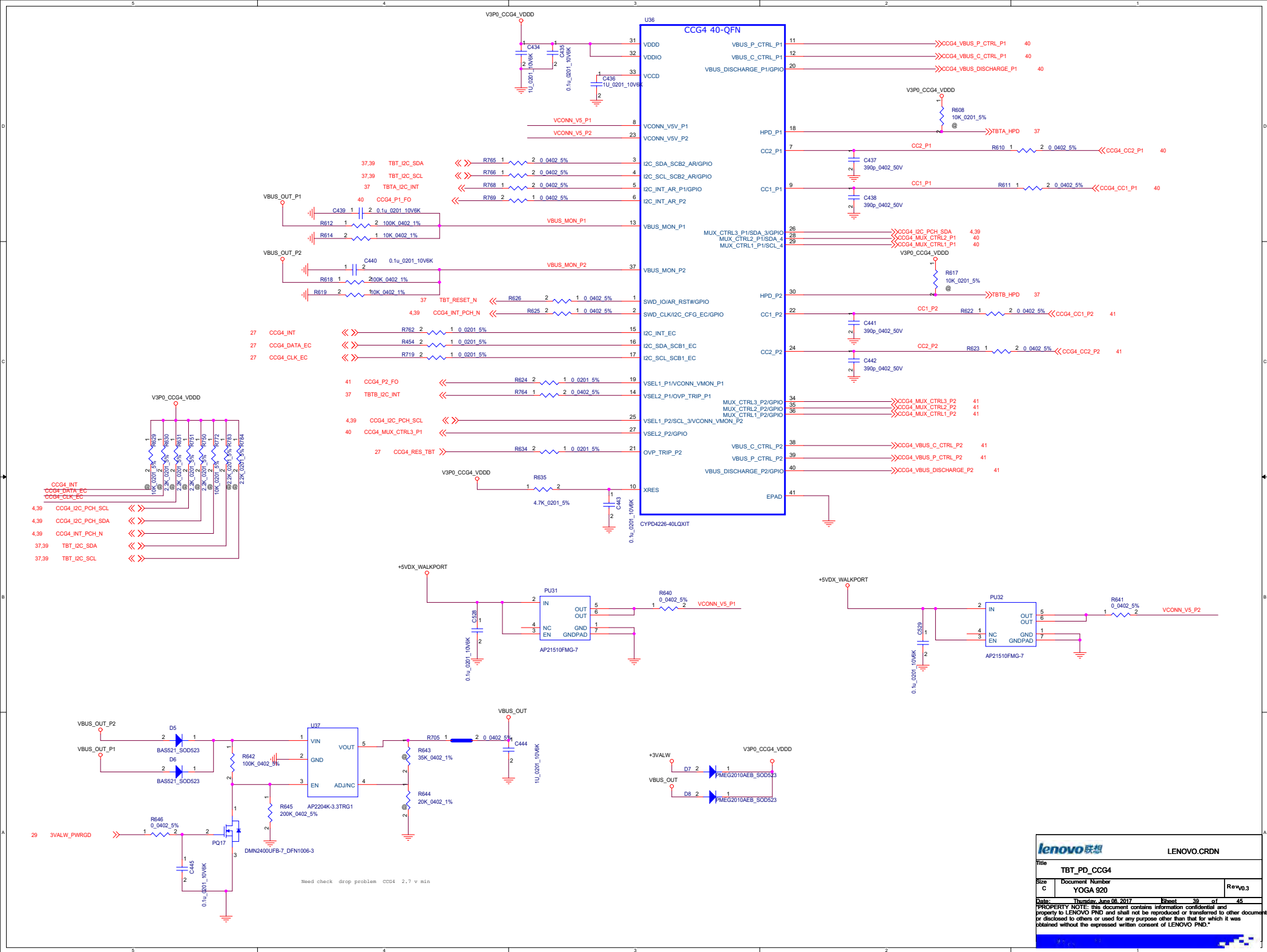
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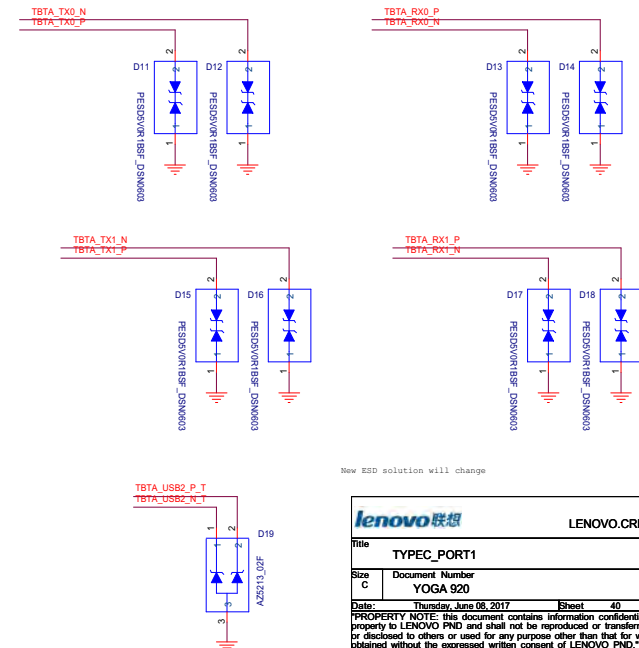
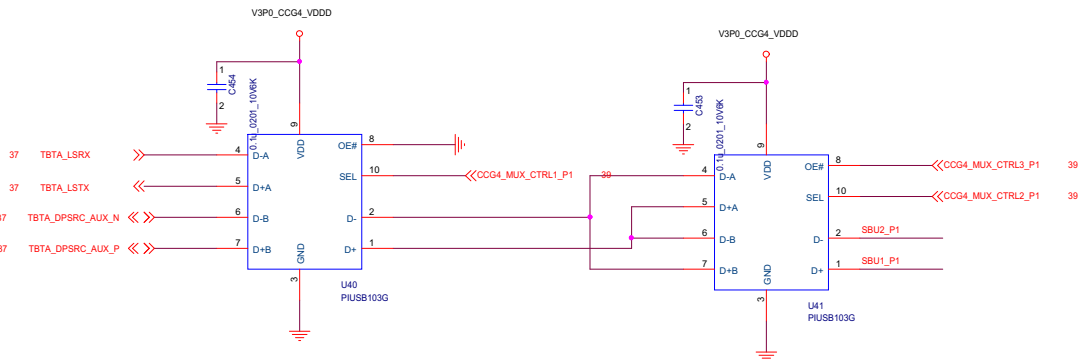
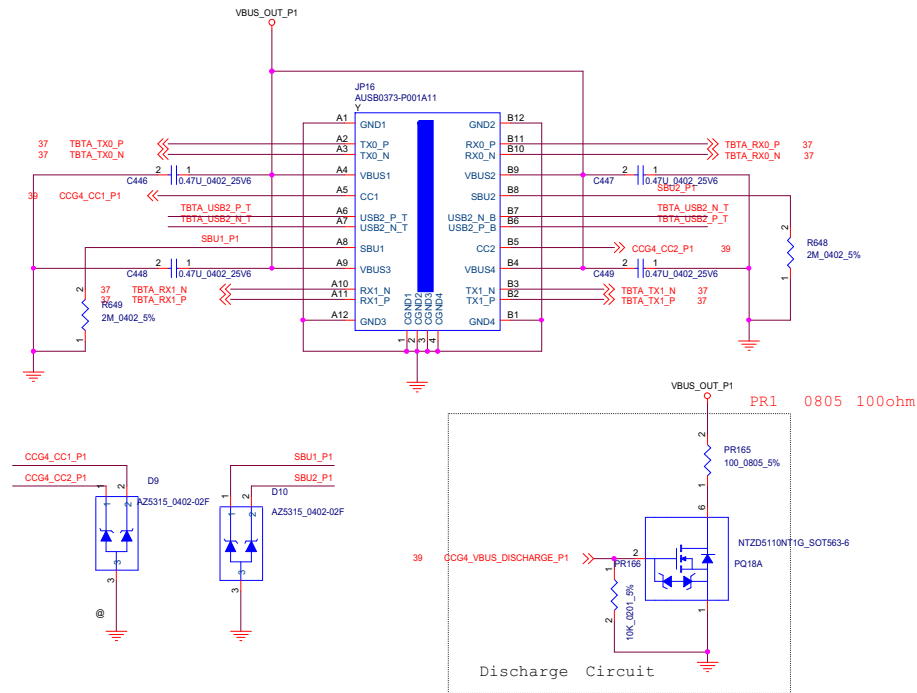
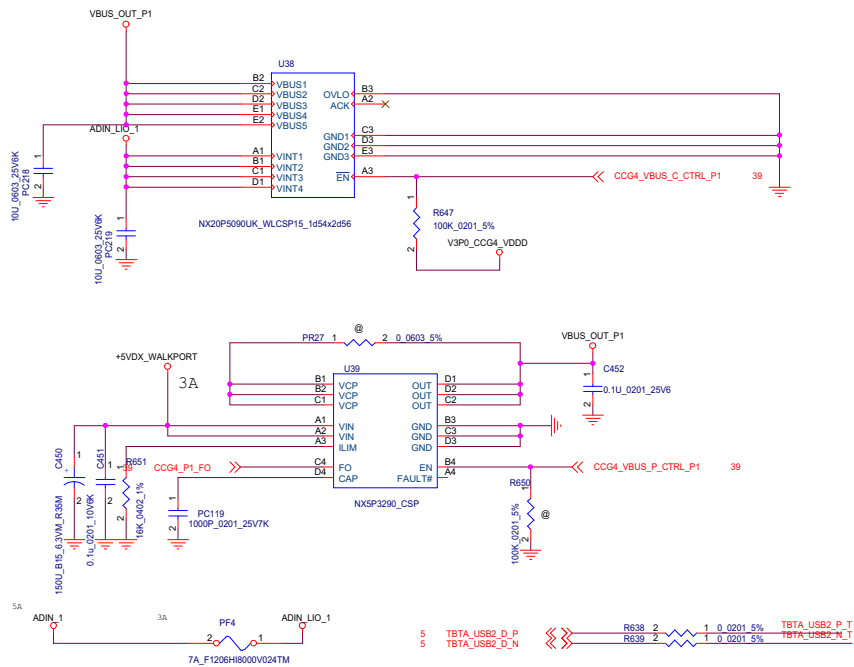
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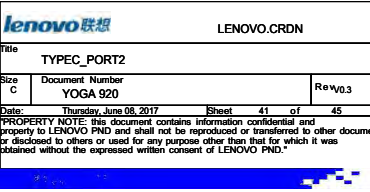
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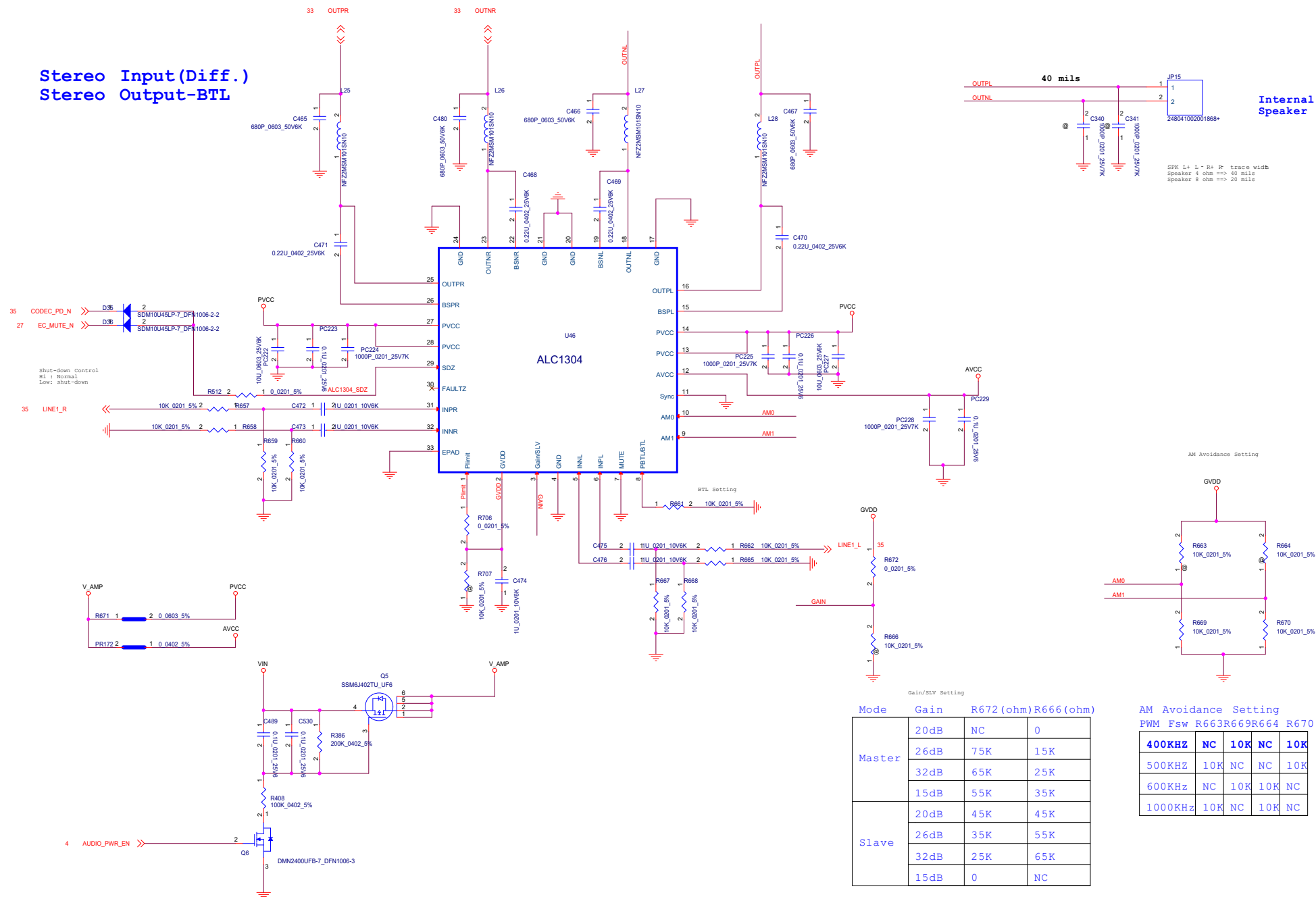


New ESD solution will change

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Title TYPEC_PORT1			
Size C	Document Number YOGA 920	Rev0.3	
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Stereo Input (Diff.)
Stereo Output-BTL



Note:
Pin29 SDZ and Pin30 FAULTZ can't be tied together

The image shows the Lenovo Smart-AMP logo on the left. To its right is a table with the following content:

LENOVO.CRDN		
Title	SMART-AMP	
Size	Document Number	Rev
C	YOGA 920	v0.3
Date	Version	Sheet
2016.10.18	001	45

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Iphone headset normal open

